REMARKS

Claims 1-22 are pending in this application, of which Claims 1, 7, 12, 14, and 18 are the independent claims. All claims stand rejected.

Summary of the Interview

Applicant thanks Examiner for the telephone interview conducted on May 2, 2008, at which Examiner Foud, Attorney James Smith and associate Benjamin Sparrow were present. During the interview, Applicant presented amendments to the claims as now provided in this Amendment. It was agreed that the amended claims distinguish over the cited references, but that an additional prior art search may be required.

In the previous Amendment filed December 3, 2007, Applicants submitted that Claims 14-17 were directed to an invention that is distinct from that of Claims 1-13 and 18-21, and suggested a Restriction of the pending claims. In order to expedite consideration of Claims 1-13 and 18-21, Claims 14-17 are being cancelled. Applicants reserve the right to file the cancelled claims in a continuation or divisional application claiming priority to the present application.

Claim 1 is being amended to further clarify the scope of the claims by reciting that "each of the serial registers" is "configured for receiving packet data from the associated input port concurrent with writing other packet data to the memory array." Claim 12 is being amended in a similar manner, by reciting that the serial registers are "configured for receiving packet data from the associated input port concurrent with writing other packet data to the memory array." Support for these amendment is found at least on page 13, lines 10-22 of the specification as originally filed. Acceptance is respectfully requested.

Objections to the Specification

The Abstract of the disclosure has been objected to for failing to describe the claimed subject matter. Accordingly, the Abstract is being revised to describe the claimed subject matter. Support for these amendments is found at least on page 12, line 24 – page 14, line 22 of the Specification as originally filed. Acceptance is respectfully requested.

Rejection of Claims 1-21 under 35 U.S.C. 102(b) and 35 U.S.C. 103(a)

Claim 14 has been rejected under 35 U.S.C. 102(b) as being anticipated by Toda et al. (U.S. Patent No. 5,612,925). Claims 15-17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Toda in view of Zuravleff et al. (U.S. Patent No. 5,867,735). Claims 14-17 are being cancelled; acceptance is respectfully requested.

Claims 1-13 and 18-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Joffe (U.S. Patent No. 5,440,523) in view of one or more of Toda and Zuravleff Applicants respectfully disagree with these rejections and request reconsideration.

Claim 1 is directed to a packet buffer random access memory (PBRAM) device. An example PBRAM device is illustrated in Fig. 7 and is not intended to limit the scope of the invention, being defined by the claims. Here, the PBRAM device 62 includes a memory array 74, a plurality of input ports 70 (I/O Port 0 – I/O Port 31), and a plurality of serial registers 72 associated with the input ports 70 (serial register 0 – serial register 31). The serial registers 72 each receive packet data from one of the associated ports 70 and write the packet data to the memory array 74 (see Specification, page 4, lines 3-11). Each of the serial registers 72 is further segmented into a plurality of segments, each segment being associated with corresponding portions of the memory array 74. Such a configuration is illustrated in Fig. 8, where a serial register 72 is divided into segments of 256 bits each. Further, a segment of the serial register 72 may transfer data into the memory 74 concurrent with another segment of the serial register 72 receiving other data (page 13, lines 11-15).

Joffe does not disclose a "plurality of serial registers...configured for receiving packet data from the associated input port concurrent with writing other packet data to the memory array" as now recited in amended Claim 1. Joffe describes a multi-port memory system. In Fig. 1 of Joffe, a number of ports (Port 1...Port k) connect to associated Memory Access Buffers, which in turn connect to a shared memory via a common bus. Joffe assigns a time slot to each port, "during which data can be read from or written to the shared memory" (col. 1, lines 36-38). During a "write" operation, all of the data stored in an associated buffer are written to the shared memory (col. 2, lines 36-44). The buffers, therefore, cannot receive data concurrent with writing data because the buffers only have a capacity to read or write at a given time. A separate "receive" operation occurs at a different time, which is prior to the write operation (col. 2, lines

17-24). Thus, Joffe does not disclose "receiving packet data from the associated input port concurrently with writing other packet data to the memory array" as now recited in amended claim 1.

Moreover, neither Joffe nor Toda disclose "segments of different serial registers simultaneously transferring packet data to different portions of the memory array," as recited in Claim 1. The Office Action asserts that Toda at Fig. 16 and col. 12, lines 8-12, teaches such a system. However, Toda at Fig. 16 discloses a single "serial register section" 167 that is associated with a single port 164, and is divided into eight "serial registers" (col. 12, lines 16-20). It should be noted that Toda's serial register section 167 is comparable to Applicant's serial register 72 (Fig. 7) because it is associated with a single port 164. Likewise, Toda's "serial registers" are comparable to Applicant's segments of the serial register 72 (Fig. 7) because they are all associated with the same port 164. Although Toda's segments transfer data to the memory 162 simultaneously, there are no different serial registers for simultaneously transferring packet data, as recited in Claim 1. In contrast, Applicants describe, in Fig. 7, multiple different serial registers 72 (32 in total) that can simultaneously transfer segments of each into the memory array 74.

Applicants agree with the Office Action in that Joffe also does not disclose the above feature. In Joffe, each buffer is assigned a time slot during which it can read from or write to the memory (col. 1, lines 36-38). The time slots for each port cannot occur simultaneously, at least because all buffers share a common bus to the memory that can accommodate only one operation at a time (col. 1, lines 20-29). Thus, Joffe and Toda fail to disclose "segments of different serial registers simultaneously transferring packet data to...the memory array" as recited in Claim 1.

For at least the reasons above, no combination of Joffe and Toda teaches or suggests the invention as recited in Claims 1, 7 and 18, as well as amended base claim 12. Claims 2-6, 8-11, 13, and 19-21 depend from one of claims 1, 7, 12 and 18, and so inherit the limitations of those claims. As a result, the §103 rejection of claims 1-13 and 18-21 is believed to be overcome, and reconsideration is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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